CAN-Transceiver Data Register Map

MODBUS Slave RTU

V1.40

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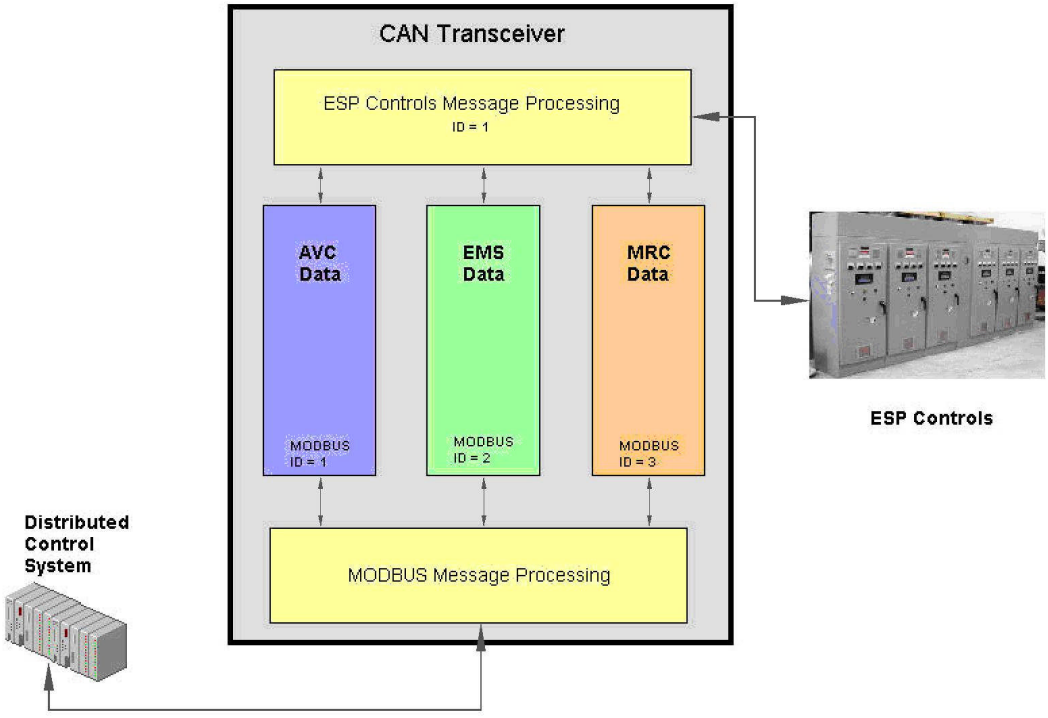
MODBUS Slave RTU CAN-Transceiver Data Register Map

Introduction

The CAN-Transceiver acts as three MODBUS slave devices in one controller. The CAN Transceiver communicates with the precipitator controls and stores data locally dependent on the type of equipment. When it communicates with the T/R controls, data is stored in the AVC Data area and rapper control data is saved in the MRC Data storage area, etc. In order for the CAN Transceiver to communicate to the ESP controls, an ID must be selected from the CAN Transceiver's keypad. Selecting the ID automatically sets the MODBUS IDs for the three data areas. The MODBUS ID for the AVC Data area will be identical to the CAN Transceiver ID. The MODBUS ID for the EMS Data area will be the CAN Transceiver ID plus one. The MODBUS ID for the MRC Data area will be the CAN Transceiver ID plus two. The figure below shows a pictorial representation of the CAN Transceiver and the data flow internal and to external equipment.



The following information is to be used by a programmer to determine the data location for the automatic voltage control (AVC), energy management system (EMS) and rapper controller (MRC) set points and data. A few registers are provided for global diagnostics as shown in the Global Data section. A base address for each device is given, and when combined with an appropriate offset determines the absolute register address.

MODBUS Protocol

The protocol used for communication with the DCS is MODBUS. Only the binary form of the MODBUS protocol, remote terminal unit (RTU) framing is supported. The DCS must be configured as the MODBUS master. The CAN-Transceiver is configured as a MODBUS slave. The following MODBUS commands are supported by the CAN-Transceiver:

READ COIL STATUS (COMMAND BYTE = 01H)
READ INPUT STATUS (COMMAND BYTE = 02H)
READ HOLDING REGISTERS (COMMAND BYTE = 03H)
FORCE SINGLE COIL (COMMAND BYTE = 05H)
WRITE SINGLE REGISTER (COMMAND BYTE = 06H)
FORCE MULTIPLE COILS (COMMAND BYTE = 0FH)
WRITE MULTIPLE REGISTERS (COMMAND BYTE = 10H)

The electrical connection to the DCS is RS232 using 8 bits, even/odd parity and 1 stop bit. The data rate is selectable from 4800, 9600, and 19200 BPS.

The DCS must not continuously transmit the write commands (05h, 06H, 0FH or 10H) to the CAN-Transceiver. A write command received by the CAN-Transceiver interrupts the communications to the local devices to prevent data update conflicts. Continuous write commands can result in a continuous interruption in local device communication.

CAN Transceiver Global Data

Holding registers 40001-40200 are Read Registers, except for some VI Plot registers. These VI Plot Resisters are explained in the VI Plot section. The MODBUS slave ID is the same as programmed for the Transceiver ID.

40001	Message Counter
40002	Read register (03) message counter
40003	Invalid CRC message counter
40004	Exception response message counter
40005	Write command message counter
40006-50	Reserved
40051	Optional digital input 1
40052	Optional digital input 2
40053	Optional digital input 3
40054	Optional digital input 4
40055	Optional digital input 5
40056	Optional digital input 6
40057	Optional digital input 7
40058	Optional digital input 8
40059-99	Reserved
40100-139	VI Plot registers
40140-200	Reserved

Optional Digital Inputs

The CAN-Transceiver has an option that allows eight 120 Vac inputs to be connected. The state of these inputs can then be read using the MODBUS address used for the AVC's. Registers 40051-40058 hold the state of the digital input. The register value 1 represents 120 V is present. The value 0 represents 120 V is not present.

AVC (TR Control) Register Base Addresses

The holding register base address shown below must be added to the MODBUS Register Offset to determine the actual register address.

Register Base Address	Device
40200	AVC #1
40400	AVC #2
40600	AVC #3
40800	AVC #4
41000	AVC #5
41200	AVC #6
41400	AVC #7
41600	AVC #8
41800	AVC #9
42000	AVC #10
42200	AVC #11
42400	AVC #12
42600	AVC #13
42800	AVC #14
43000	AVC #15
43200	AVC #16
43400	AVC #17
43600	AVC #18
43800	AVC #19
44000	AVC #20
44200	AVC #21
44400	AVC #22
44600	AVC #23
44800	AVC #24

As an example, the primary voltage reading (offset 07) for AVC number 3 (base 40600) is register 40607.

AVC MODBUS Register Definition

Registers offset 01-100 are read only registers

Offset from base address		
01	AVC Status Word 1	
	Bit 0 Running	(Set when in run mode)
	Bit 1 Stand alone	(Set when operating in stand alone mode)
	Bit 2 Manual	(Set when operating in manual mode)
	Bit 3 Continuous	(Set when operating in Continuous mode)
	Bit 4 IE	(Set when operating in I.E. mode)
	Bit 5 BC	(Set when back corona detected mode)
	Bit 6 IE optimise	(Set when operating in I.E. optimise mode)
	Bit 7 Reserved	

	Bit 8 Reserved	
	Bit 9 Contactor open	(Set when contactor is open)
	Bit 10 Wash down	(Set when WESP wash down is active)
	Bit 11 Relay 1	(Set when relay 1 is energized)
	Bit 12 Relay 2	(Set when relay 2 is energized)
	Bit 13 Relay 3	(Set when relay 3 is energized)
	Bit 14 Relay 4	(Set when relay 4 is energized)
	Bit 15 Reserved	
02	AVC Status Word 2	
	Bit 0 Reserved	
	Bit 1 Reserved	
	Bit 2 Reserved	
	Bit 3 Vs Limit	(Set when Vs limit operational)
	Bit 4 Is Limit	(Set when Is Limit operational)
	Bit 5 Vp Limit	(Set when Vp Limit operational)
	Bit 6 Ip Limit	(Set when Ip Limit operational)
	Bit 7 UV	(Set during under voltage condition)
	Bit 8 Is Pk Limit	(Set when Is peak limit is operational)
	Bit 9 Vs Rap Limit	(Set when power down rapping vs limit operational)
	Bit 10-14 Reserved	
	Bit 15 Comm. Error	(Set during AVC communications error)
03	Reserved	
04	AVC Alarm Word	(Set = alarm)
	Bit 0 Over current trip	
	Bit 1 Thyristor (SCR) unbalance	
	Bit 2 Under voltage trip	
	Bit 3 Zero Cross Fault	
	Bit 4 Coordination error	
	Bit 5 MRC Comm. Error (power down rapping)	
	Bit 6 External Alarm 1	
	Bit 7 External Alarm 2	
	Bit 8 External Alarm 3	
	Bit 9 External Alarm 4	
	Bit 10-14 Reserved	
	Bit 15 Common Alarm	
05	Reserved	
06	Reserved	
07	Primary Voltage value	0-600 Volts
08	Primary Current value	0 – 500 Amperes
09	Primary Power value	kW
10	Secondary Voltage value	0-99 kV1
11	Secondary Voltage value	0-99 kV2
12	Secondary Current value	0-3000 ma
13	Sparks per minute value	0-999
14	Arcs per minute value	0-999
15-100	Reserved	

Register offsets in the range of 101 to 200 are read/write registers, except for register offsets 110, 124 and 125 that are read only.

101	Control Word	
	Bit 0 Start	(Set to start)
	Bit 1 Alarm reset	(Set to reset alarm. See Note)
	Bit 2 Spark rate mode	(Set to enable spark rate mode)
	Bit 3 IE Enable	(Set to enable IE mode)
	Bit 4 IE optimise mode	(Set to I.E. enable optimise mode,)
	Bit 5-15 reserved	
102	Reserved	
103	Program Number for Rapper	(1-6)
104	Primary Voltage Limit	(1-600 Volts)
105	Primary Current Limit	(1-500 Amperes)
106	Secondary Voltage Limit	(1-99 kV)
107	Secondary Current Limit	(1-3000 ma)
108	Under voltage set point	(20-300 Volts OR 5-99 kV)
109	Secondary Current Peak Limit	(ma)
110	Under voltage trip mode	(0= Primary voltage, 1 = Secondary voltage)
111	Reserved	
112	Ramp	(2-600 $\rightarrow$ 0.2-60.0 seconds)
113	Phase Back	(1-99 %)
114	Pedestal	(1-10 cycles)
115	Quench time	(1-9 cycles)
116	Spark Rate	(2-200 sparks per minute)
117	Reserved	
118	IE Charge half cycles	(1-30 half cycles)
119	IE Discharge cycles	(1-32 cycles)
120	IE Background power	(0-50%)
121	IE Optimise Timer	(5-180 minutes)
122	Power Down Rapping	(0-99 kV)
123	Rapper Control Word	
	Bit 0 Rapper 1 Enable	(Set to enable rapper relay 1)
	Bit 1 Rapper 2 Enable	(Set to enable rapper relay 2)
	Bit 2 Rapper 3 Enable	(Set to enable rapper relay 3)
	Bit 3 Rapper 4 Enable	(Set to enable rapper relay 4)
	Bit 4 Master enable	(Set to globally enable rapper relays)
	Bit 5 Rapper 1 PwrDown	(Set to enable power down rapping on relay 1)
	Bit 6 Rapper 2 PwrDown	(Set to enable power down rapping on relay 2)
	Bit 7 Rapper 3 PwrDown	(Set to enable power down rapping on relay 3)
	Bit 8 Rapper 4 PwrDown	(Set to enable power down rapping on relay 4)
	Bit 9-15 reserved	
124	Rapper Mode Word 1	
	Bit 0-7 Rapper Queue 1	(Rapper 1 queue, 0-2)
	Bit 8-15 Rapper Queue 2	(Rapper 2 queue, 0-2)
125	Rapper Mode Word 2	
	Bit 0-7 Rapper Queue 3	(Rapper 3 queue, 0-2)
	Bit 8-15 Rapper Queue 4	(Rapper 4 queue, 0-2)
126	Rapper 1 Interval Timer	(1-64800 seconds)
127	Rapper 1 On Timer	(1-64800 seconds)
128	Rapper 2 Interval Timer	(1-64800 seconds)
129	Rapper 2 On Timer	(1-64800 seconds)
130	Rapper 3 Interval Timer	(1-64800 seconds)
131	Rapper 3 On Timer	(1-64800 seconds)
132	Rapper 4 Interval Timer	(1-64800 seconds)
133	Rapper 4 On Timer	(1-64800 seconds)
134-201	Reserved	

Note:

The alarm reset (bit 1) of the Control Word (offset 101) resets the AVC alarm status. The Transceiver will automatically clear this bit after it sends an alarm reset command to the AVC.

VI Plot Registers

The transformer/rectifier control is capable of automatically collecting data for a V/I curve. Only one set of registers is used for this data in the 40100 to 40144 register range.

Register	Definition
40100	Requested AVC ID for V/I plot. DCS writes this register to begin the VI plot data collection. This register is automatically zeroed when VI plot is complete
40101	When a plot is started, the AVC ID from register 40100 is copied into this register. It is not cleared when the plot is complete.
40102	VI plot status flag. 1=plot started, 2= plot complete, 8=error
40103	Number of readings taken for VI plot.
40104	While a plot is being taken this register is zero. After a plot is complete, this register holds the secondary current value that is used as the increment when taking data for a VI plot. This value will be equal to: (Ending_Is_Limit – Starting_Is_Limit) / 14
40105	Starting Secondary Current Limit (Must be greater than 24 ma)
40106	Ending Secondary Current Limit (Must be at least 375 ma greater than the starting secondary current limit)
40107-40109	Reserved
40110	VI plot kV reading 1
40111	VI plot kV reading 2
40112	VI plot kV reading 3
40113	VI plot kV reading 4
40114	VI plot kV reading 5
40115	VI plot kV reading 6
40116	VI plot kV reading 7
40117	VI plot kV reading 8
40118	VI plot kV reading 9
40119	VI plot kV reading 10
40120	VI plot kV reading 11
40121	VI plot kV reading 12
40122	VI plot kV reading 13
40123	VI plot kV reading 14
40124	VI plot kV reading 15
40125-40129	Reserved
40130	VI plot kV Min. reading 1
40131	VI plot kV Min. reading 2
40132	VI plot kV Min. reading 3
40133	VI plot kV Min. reading 4
40134	VI plot kV Min. reading 5
40135	VI plot kV Min. reading 6
40136	VI plot kV Min. reading 7
40137	VI plot kV Min. reading 8
40138	VI plot kV Min. reading 9
40139	VI plot kV Min. reading 10
40140	VI plot kV Min. reading 11
40141	VI plot kV Min. reading 12
40142	VI plot kV Min. reading 13
40143	VI plot kV Min. reading 14
40144	VI plot kV Min. reading 15

Due to operating characteristics, the AVC control may not be able to take 15 readings. Register 40102 should be used to determine the actual number of readings that were taken.

AVC Input Status Base Addresses

The CAN Transceiver offers an alternative binary addressing mode for reading the AVC Status Word 1, AVC Status Word 2, and the AVC Alarm Word. The MODBUS function Read Input Status (function 02) for discrete inputs (1x references) is supported. The Input Status base address shown below must be added to the Input Status Offset to determine the actual address.

Input Status Base Address	Device
10000	AVC #1
10064	AVC #2
10128	AVC #3
10192	AVC #4
10256	AVC #5
10320	AVC #6
10384	AVC #7
10448	AVC #8
10512	AVC #9
10576	AVC #10
10640	AVC #11
10704	AVC #12
10768	AVC #13
10832	AVC #14
10896	AVC #15
10960	AVC #16
11024	AVC #17
11088	AVC #18
11152	AVC #19
11216	AVC #20
11280	AVC #21
11344	AVC #22
11408	AVC #23
11472	AVC #24

As an example, the Comm. Error status (offset 32) for AVC number 3 (base 10128) is input status 10160.

AVC MODBUS Input Status Definition

Offset from base address	Definition	
	AVC Status Word 1	
1	Bit 0 Running	(Set when in run mode)
2	Bit 1 Stand alone	(Set when operating in stand alone mode)
3	Bit 2 Manual	(Set when operating in manual mode)
4	Bit 3 Continuous	(Set when operating in Continuous mode)
5	Bit 4 IE	(Set when operating in I.E. mode)
6	Bit 5 BC	(Set when back corona detected mode)
7	Bit 6 IE optimize	(Set when operating in I.E. optimize mode)
8	Bit 7	Reserved
9	Bit 8	Reserved
10	Bit 9 Contactor open	(Set when contactor is open)
11	Bit 10 Wash down	(Set when WESP wash down is active)
12	Bit 11 Relay 1	(Set when relay 1 is energized)
13	Bit 12 Relay 2	(Set when relay 2 is energized)
14	Bit 13 Relay 3	(Set when relay 3 is energized)
15	Bit 14 Relay 4	(Set when relay 4 is energized)
16	Bit 15	Reserved
	AVC Status Word 2	
17-19	Bit 0 -2	Reserved
20	Bit 3 Vs Limit	(Set when Vs limit operational)
21	Bit 4 Is Limit	(Set when Is Limit operational)
22	Bit 5 Vp Limit	(Set when Vp Limit operational)
23	Bit 6 Ip Limit	(Set when Ip Limit operational)
24	Bit 7 UV	(Set during under voltage condition)
25	Bit 8 Is Pk Limit	(Set when Is peak limit is operational)
26	Bit 9 Vs Rap Limit	(Set when power down rapping Vs limit operational)
27-31	Bit 10-14	Reserved
32	Bit 15 Comm. Error	(Set during AVC communications error)
33-48	Bit 0-15 Reserved	
	AVC Alarm Word	
49	Bit 0 Over current trip	
50	Bit 1 Thyristor (SCR) unbalance	
51	Bit 2 Under voltage trip	
52	Bit 3 Zero Cross Fault	
53	Bit 4 Coordination error	
54	Bit 5 MRC Comm. Error	(for power down rapping)
55	Bit 6 External Alarm 1	
56	Bit 7 External Alarm 2	
57	Bit 8 External Alarm 3	
58	Bit 9 External Alarm 4	

59-63	Bit 10-15 Reserved
64	Bit 15 Common alarm

AVC Coil Base Addresses

The CAN Transceiver offers an alternative binary addressing mode for reading and writing the AVC Control Word. The MODBUS function Read Coil Status (function 01) and Force Single Coil (function 05) for discrete outputs (0x references) is supported. The Coil Status base address shown below must be added to the Coil Status Offset to determine the actual address.

Coil Base Address	Device
00000	AVC #1
00016	AVC #2
00032	AVC #3
00048	AVC #4
00064	AVC #5
00080	AVC #6
00096	AVC #7
00112	AVC #8
00128	AVC #9
00144	AVC #10
00160	AVC #11
00176	AVC #12
00192	AVC #13
00208	AVC #14
00224	AVC #15
00240	AVC #16
00256	AVC #17
00272	AVC #18
00288	AVC #19
00304	AVC #20
00320	AVC #21
00336	AVC #22
00352	AVC #23
00368	AVC #24

As an example, the Spark Rate Mode coil (offset 3) for AVC number 3 (base 32) is coil 35.

AVC MODBUS Coil Definition

Offset from base address	Definition	
	Control Word	
1	Bit 0 Start	(Set to start)
2	Bit 1 Alarm reset	(Set to reset alarm. See Note 1.)
3	Bit 2 Spark rate mode	(Set to enable spark rate mode)
4	Bit 3 IE Enable	(Set to enable IE mode)
5	Bit 4 IE optimize mode	(Set to I.E. enable optimize mode)
6-16	Bit 5-15	Reserved

Energy Management System

Energy Management System Register Base Addresses

The holding register base address shown below must be added to the MODBUS Register Offset to determine the actual register address. The MODBUS slave ID is the same as programmed for the Transceiver ID + 1.

Register Base Address	Device
40100	EMS #1
40200	EMS #2
40300	EMS #3
40400	EMS #4

Energy Management MODBUS Register Definition

Register offsets 1 to 4 are read only registers if the opacity signal is being brought directly into the CAN-Transceiver as an analog signal. They are write only registers if the opacity signal is being brought into the CAN-Transceiver through the communications link.

Register offset 5 is a read or write register.
Register offsets 6 to 50 are read only registers.

Offset from Base address		
1	Opacity	(0-100 %)
2	Reserved	
3	Reserved	
4	Opacity Status Word	
	Bit 0 Calibrate	(Set when in calibrate mode)
	Bit 1 Failed	(Set when opacity signal failed)
	Bit 2-15 reserved	
5	EMS Control Word	
	Bit 0 Enable/Disable	(Set to enable EMS)
	Bit 1 Power mode	(Set for power mode, cleared for IE mode)
	Bit 2 Series mode	(Set for series mode, cleared for parallel mode)
	Bit 3 Limit mode	(Set for limit mode, See Note 1)
	Bit 4-15 reserved	
6	Reserved	
7	Lower Limit	(0-100)
8	Upper Limit	(0-100)
9	Hours	(1-24)
10	Rate of Change	(1-9)
11	Adjustment Delay	(1-999 seconds)
12	Reserved	
13	Reserved	

14	Reserved	
15	Field 1 Minimum Power	(0-100 %)
16	Field 1 Maximum IE value	(0-23, See note 2)
17	Field 1 Sequence Number	(1-6)
18	Field 1 EMS value	(See note 3)
19	Reserved	
20	Reserved	
21	Field 2 Minimum Power	(0-100 %)
22	Field 2 Maximum IE value	
23	Field 2 Sequence Number	(1-6)
24	Field 2 EMS value	
25	Reserved	
26	Reserved	
27	Field 3 Minimum Power	(0-100 %)
28	Field 3 Maximum IE value	
29	Field 3 Sequence Number	(1-6)
30	Field 3 EMS value	
31	Reserved	
32	Reserved	
33	Field 4 Minimum Power	(0-100 %)
34	Field 4 Maximum IE value	
35	Field 4 Sequence Number	(1-6)
36	Field 4 EMS value	
37	Reserved	
38	Reserved	
39	Field 5 Minimum Power	(0-100 %)
40	Field 5 Maximum IE value	
41	Field 5 Sequence Number	(1-6)
42	Field 5 EMS value	
43	Reserved	
44	Reserved	
45	Field 6 Minimum Power	(0-100 %)
46	Field 6 Maximum IE value	
47	Field 6 Sequence Number	(1-6)
48	Field 6 EMS value	
49-100	Reserved	

Notes:

1. This bit is always set.

2. The Maximum IE value is an index into a table to provide the number of charge half cycles and discharge cycles. See the IE Index Map Table below.

3. The EMS value depends on the EMS mode. In power mode, the EMS value represents the target power level in percent from 0 to 100. In IE mode, the EMS value represents an index into the IE Index Map Table as follows:

IE Index	IE Charge ½ Cycles	IE Discharge Cycles
0	32	0
1	30	1
2	28	1
3	26	1
4	24	1
5	22	1
6	20	1
7	18	1
8	16	1
9	14	1
10	12	1
11	10	1
12	8	1
13	6	1
14	4	1
15	2	1
16	2	2
17	2	3
18	2	4
19	2	5
20	2	6
21	2	7
22	2	8
23	2	9

IE Index Map Table

Microprocessor Rapper Control (MRC)

MRC (Rapper Control) Register Base Addresses

The holding register base address shown below must be added to the MODBUS Register Offset to determine the actual register address. The MODBUS slave ID is the same as programmed for the Transceiver ID + 2.

Register Base Address	Device
40000	MRC #1
41000	MRC #2
42000	MRC #3
43000	MRC #4

MRC MODBUS Register Definition

Register offsets 1 to 200 are read registers.
Register offsets 201 to 1000 are read/write registers.

Offset from Base address		
1	MRC Status Word 1	
	Bit 0 Running	(Set when in run mode)
	Bit 1 Stand alone	(Set when operating in stand alone mode)
	Bit 2 Sequence Mode	(Set when operating in sequence)
	Bit 3 Repeat Mode	(Set when operating in repeat)
	Bit 4-7 Reserved	
	Bit 8 Disabled Clock	(Set when a clock is disabled)
	Bit 9 Disabled Device	(Set when a device is manually disabled)
	Bit 10-11 Reserved	
	Bit 12 Low Level Alarm	(Set when a device has a low level alarm)
	Bit 13 Med. Level Alarm	(Set when a device has medium level alarm)
	Bit 14 High Level Alarm	(Set when a device has a high level alarm)
	Bit 15 Comm. Error	(Set during MRC communications error)
2	MRC Status Word 2	
	Bit 0 Input 1	(Set when digital input 1 is high)
	Bit 1 Input 2	(Set when digital input 2 is high)
	Bit 2 Input 3	(Set when digital input 3 is high)
	Bit 3 Input 4	(Set when digital input 4 is high)
	Bit 4 Output 1	(Set when digital output 1 is high)
	Bit 5 Output 2	(Set when digital output 2 is high, Run status)
	Bit 6 Output 3	(Set when digital output 3 is high, NOT Fault)
	Bit 7 Output 4	(Set when fault relay NO is closed)
	Bit 8-15 Reserved	
3	Firing Device Number	
4	Firing Device Number	
5	Reserved	

6	Program Number	(1-6, Read only)	
7	Reserved		
8	Total number of clocks		
9	Total number of devices		
10	Number of Disabled Devices	See note 10	
11	Device Alarm 1 – 4	See note 1	
12	Device Alarm 5 – 8		
13	Device Alarm 9 - 12		
14	Device Alarm 13 - 16		
15	Device Alarm 17 - 20		
16	Device Alarm 21 - 24		
17	Device Alarm 25 – 28		
18	Device Alarm 29 – 32		
19	Device Alarm 33 - 36		
20	Device Alarm 37 - 40		
21	Device Alarm 41 - 44		
22	Device Alarm 45 – 48		
23	Device Alarm 49 - 52		
.	.		
.	.		
138	Device Alarm 509 – 512		
139-200	Reserved		
201	Control Word		
	Bit 0 Start	(Set to start)	
	Bit 1 reserved		
	Bit 2 Sequence all	(Set to sequence all devices)	
	Bit 4 Abort PDR	(Set to abort PDR cycle)	
	Bit 3-15 reserved		
202	Clock Enable 1	Clocks 1-16	See note 2
203	Clock Enable 2	Clocks 17-32	
204	Clock Enable 3	Clocks 33-48	
205	Clock Enable 4	Clocks 49-63	
206	Reserved		
207	Program Number	(1-6)	See note 3
208	Reserved		
209	Cycle Clock 1 – hours	(0-99)	
210	Cycle Clock 1 – seconds	(0 to 3,599)	See note 4
211	Wait Clock 1 – hours	(0-99)	See note 5
212	Wait Clock 1 – seconds	(0 to 3,599)	See note 5 & 6
213	Cycle Clock 2 – hours	(0-99)	
214	Cycle Clock 2 – seconds	(0 to 3,599)	
215	Wait Clock 2 – hours	(0-99)	
216	Wait Clock 2 – seconds	(0 to 3,599)	
217	Cycle Clock 3 – hours	(0-99)	
218	Cycle Clock 3 – seconds	(0 to 3,599)	
219	Wait Clock 3 – hours	(0-99)	
220	Wait Clock 3 – seconds	(0 to 3,599)	
221	Cycle Clock 4 – hours	(0-99)	
222	Cycle Clock 4 – seconds	(0 to 3,599)	
223	Wait Clock 4 – hours	(0-99)	
224	Wait Clock 4 – seconds	(0 to 3,599)	
225	Cycle Clock 5 – hours	(0-99)	
226	Cycle Clock 5 – seconds	(0 to 3,599)	
227	Wait Clock 5 – hours	(0-99)	
228	Wait Clock 5 – seconds	(0 to 3,599)	

229	Cycle Clock 6 – hours	(0-99)	
230	Cycle Clock 6 – seconds	(0 to 3,599)	
231	Wait Clock 6 – hours	(0-99)	
232	Wait Clock 6 – seconds	(0 to 3,599)	
233	Cycle Clock 7 – hours	(0-99)	
234	Cycle Clock 7 – seconds	(0 to 3,599)	
235	Wait Clock 7 – hours	(0-99)	
236	Wait Clock 7 – seconds	(0 to 3,599)	
237	Cycle Clock 8 – hours	(0-99)	
238	Cycle Clock 8 – seconds	(0 to 3,599)	
239	Wait Clock 8 – hours	(0-99)	
240	Wait Clock 8 – seconds	(0 to 3,599)	
241	Cycle Clock 9 – hours	(0-99)	
242	Cycle Clock 9 – seconds	(0 to 3,599)	
243	Wait Clock 9 – hours	(0-99)	
244	Wait Clock 9 – seconds	(0 to 3,599)	
245	Cycle Clock 10 – hours	(0-99)	
246	Cycle Clock 10 – seconds	(0 to 3,599)	
247	Wait Clock 10 – hours	(0-99)	
248	Wait Clock 10 – seconds	(0 to 3,599)	
249	Cycle Clock 11 – hours	(0-99)	
250	Cycle Clock 11 – seconds	(0 to 3,599)	
251	Wait Clock 11 – hours	(0-99)	
252	Wait Clock 11 – seconds	(0 to 3,599)	
253	Cycle Clock 12 – hours	(0-99)	
254	Cycle Clock 12 – seconds	(0 to 3,599)	
255	Wait Clock 12 – hours	(0-99)	
256	Wait Clock 12 – seconds	(0 to 3,599)	
257	Cycle Clock 13 – hours	(0-99)	
258	Cycle Clock 13 – seconds	(0 to 3,599)	
259	Wait Clock 13 – hours	(0-99)	
260	Wait Clock 13 – seconds	(0 to 3,599)	
.	.		
.	.		
457	Cycle Clock 63 – hours	(0-99)	
458	Cycle Clock 63 – seconds	(0 to 3,599)	
459	Wait Clock 63 – hours	(0-99)	
460	Wait Clock 63– seconds	(0 to 3,599)	
461-500	Reserved		
501	Lift Devices 1&2	(MSB Device 1, LSB Device 2)	See note 7
502	Lift Devices 3&4	(MSB Device 3, LSB Device 4)	
503	Lift Devices 5&6	(MSB Device 5, LSB Device 6)	
504	Lift Devices 7&8	(MSB Device 7, LSB Device 8)	
505	Lift Devices 9&10	(MSB Device 9, LSB Device 10)	
506	Lift Devices 11&12	(MSB Device 11, LSB Device 12)	
507	Lift Devices 13&14	(MSB Device 13, LSB Device 14)	
508	Lift Devices 15&16	(MSB Device 15, LSB Device 16)	
509	Lift Devices 17&18	(MSB Device 17, LSB Device 18)	
510	Lift Devices 19&20	(MSB Device 19, LSB Device 20)	
511	Lift Devices 21&22	(MSB Device 21, LSB Device 22)	
512	Lift Devices 23&24	(MSB Device 23, LSB Device 24)	
513	Lift Devices 25&26	(MSB Device 25, LSB Device 26)	
514	Lift Devices 27&28	(MSB Device 27, LSB Device 28)	

515	Lift Devices 29&30	(MSB Device 29, LSB Device 30)
516	Lift Devices 31&32	(MSB Device 31, LSB Device 32)
.	.	
.	.	
755	Lift Device 509&510	(MSB Device 509, LSB Device 510)
756	Lift Device 511&512	(MSB Device 511, LSB Device 512)
757-759	Reserved	
760	Clock Intensity Change	See note 8
761	Clock 1 PD Lift	Clock 1 index for PD lift - See note 9
762	Clock 2 PD Lift	Clock 2 index for PD lift
763	Clock 3 PD Lift	Clock 3 index for PD lift
764	Clock 4 PD Lift	Clock 4 index for PD lift
765	Clock 5 PD Lift	Clock 5 index for PD lift
766	Clock 6 PD Lift	Clock 6 index for PD lift
767	Clock 7 PD Lift	Clock 7 index for PD lift
768	Clock 8 PD Lift	Clock 8 index for PD lift
769	Clock 9 PD Lift	Clock 9 index for PD lift
770	Clock 10 PD Lift	Clock 10 index for PD lift
.	.	
.	.	
823	Clock 63 PD Lift	Clock 63 index for PD lift
824-1000	Reserved	

Notes:

The MRC has a maximum capability of 63 clocks and 512 devices. Most installations will have less then the maximum. It is recommended that only data that needed be read by the master MODBUS device.

1. Four alarm codes are held in each register. The first code is stored in bits 15-12. The second alarm code is stored in bits 11-8. The third alarm code is stored in bits 7-4. The fourth alarm code is stored in bits 3-0. The alarm codes are represented in the table below:

Alarm Code	Bit pattern
No Alarm	0000
Open Circuit	0001
Medium Current	0010
Short Circuit	0100
Manually Disabled	1000

As an example, register 40013 containing the bit pattern 0100 0000 0000 0001 would indicate Device 9 has a short circuit alarm, devices 10 and 11 with no alarms and device 12 with a open circuit alarm for MRC #1.

2. Bit 0 of the clock enables register represents clock 1, bit 1 represents clock 2, etc. The remaining clock enable registers are numbered in a similar manner.

3. When making a change to the program number, no other changes must be made until the program number is updated in register offset 6. This insures data is written for the correct program.

4. Cycle Clock seconds range from 0 to 3,599. This allows the cycle clock minutes and seconds to be transferred as one MODBUS register. As an example register 40209 holds the value 2, register 40210 holds 184. This represents a time of 2 hours, 3 minutes and 4 seconds.

5. Wait Clock registers represent the ON TIME for vibrator devices.

6. Wait Clock seconds range from 0 to 3,599. This allows the wait clock minutes and seconds to be transferred as one MODBUS register.

7. Registers containing device lift hold the lift for two devices. The first device is in the most significant byte and the next device is in the least significant byte. Some MRC configurations may limit the maximum rapper lift. The value is an index into the table below:

Index Value	Rapper Lift	Vibrator Intensity
0	0.00”	n. a.
1	0.25”	n. a.
2	0.50”	n. a.
3	0.75”	n. a.
4	1.00”	n. a.
5	1.25”	n. a.
6	1.50”	n. a.
7	1.75”	n. a.
8	2.00”	n. a.
9	2.25”	n. a.
10	2.50”	50 %
11	2.75”	55 %
12	3.00”	60 %
13	3.50”	65 %
14	4.00”	70 %
15	4.50”	75 %
16	5.00”	80 %
17	5.50”	85 %
18	6.00”	90 %
19	6.50”	95 %
20	7.00”	100 %
21	7.50”	
22	8.00”	
23	8.50”	
24	9.00”	
25	9.50”	
26	10.00”	
27	10.50”	
28	11.00”	
29	12.00”	
30	13.00”	
31	14.00”	

Rapper Lift / Vibrator Intensity Table

8. The Clock Intensity Change register allows the intensity of all the devices associated with a particular cycle clock, or all the devices on the control to be increased, or decreased, at the same time. The LSB of the register specifies the cycle clock number that will have its devices adjusted. A value of zero in the LSB of this register selects all devices on the control to be adjusted. The MSB of this register specifies the size of the increase or decrease. A positive number increases the intensity and a negative number decreases the intensity. The MRC adds the MSB value to the current intensity index value for the device resulting in a new index value. The MRC insures the new intensity does not exceed the maximum configured intensity. The CAN-Transceiver will automatically clear this register to zero after the command has been sent to the MRC.

9. The Clock PD Lift registers hold the intensity for power down rapping clocks. If the associated clock is not a power down rapping clock, the register will be zero. If the associated clock is a power

down rapping clock, the register will hold an index into a table of rapper lifts/vibrator intensity. See the table from note 7 for index values.

10. The Number of Disabled Devices register holds the count of devices that are alarmed and manually disabled. This register is useful in determining the severity of alarms when customers choose not to read the alarm registers associated with individual rappers.

MRC Input Status Base Addresses

The CAN Transceiver offers an alternative binary addressing mode for reading the MRC Status Word 1 and MRC Status Word 2. The MODBUS function Read Input Status (function 02) for discrete inputs (1x references) is supported. The Input Status base address shown below must be added to the Input Status Offset to determine the actual address.

Input Status Base Address	Device
10000	MRC #1
10032	MRC #2
10064	MRC #3
10096	MRC #4

MRC MODBUS Input Status Definition

Offset from base address	Definition	
	MRC Status Word 1	
1	Bit 0 Running	(Set when in run mode)
2	Bit 1 Stand alone	(Set when operating in stand alone mode)
3	Bit 2 Sequence Mode	(Set when operating in sequence)
4	Bit 3 Repeat Mode	(Set when operating in repeat)
5-8	Bit 4-7 Reserved	
9	Bit 8 Disabled Clock	(Set when a clock is disabled)
10	Bit 9 Disabled Device	(Set when a device is manually disabled)
11	Bit 10	Reserved
12	Bit 11	Reserved
13	Bit 12 Low Level Alarm	(Set when a device has a low level alarm)
14	Bit 13 Medium Level Alarm	(Set when a device has a medium level alarm)
15	Bit 14 High Level Alarm	(Set when a device has a high level alarm)
16	Bit 15 Communication Error	(Set during MRC communications error)
	MRC Status Word 2	
17	Bit 0 Input 1	(Set when digital input 1 is high)
18	Bit 1 Input 2	(Set when digital input 2 is high)
19	Bit 2 Input 3	(Set when digital input 3 is high)
20	Bit 3 Input 4	(Set when digital input 4 is high)
21	Bit 4 Output 1	(Set when digital output 1 is high)

22	Bit 5 Output 2	(Set when digital output 2 is high)
23	Bit 6 Output 3	(Set when digital output 3 is high)
24	Bit 7 Output 4	(Set when fault relay NO is closed)
25-32	Bit 8-15	Reserved

MRC Coil Base Addresses

The CAN Transceiver offers an alternative binary addressing mode for reading and writing the MRC Control Word and Clock Enable words 1, 2, 3, and 4. The MODBUS function Read Coil Status (function 01) and Force Single Coil (function 05) for discrete outputs (0x references) is supported. The Coil Status base address shown below must be added to the Coil Status Offset to determine the actual address.

Coil Status Base Address	Device
00000	MRC #1
00096	MRC #2
00192	MRC #3
00288	MRC #4

MRC MODBUS Coil Status Definition

Offset from base address	Definition	
	Control Word	
1	Bit 0 Start	1 = Start
2	Bit 1	Reserved
3	Bit 2 Sequence All	1 = Sequence All Mode Enable
4-16	Bit 3 -16	Reserved
	Clock Enable 1	
17	Bit 0 Clock Enable 1	0 = Disabled, 1 = Enabled
18	Bit 1 Clock Enable 2	
19	Bit 2 Clock Enable 3	
20	Bit 3 Clock Enable 4	
21	Bit 4 Clock Enable 5	
22	Bit 5 Clock Enable 6	
23	Bit 6 Clock Enable 7	
24	Bit 7 Clock Enable 8	
25	Bit 8 Clock Enable 9	
26	Bit 9 Clock Enable 10	
27	Bit 10 Clock Enable 11	
28	Bit 11 Clock Enable 12	
29	Bit 12 Clock Enable 13	
30	Bit 13 Clock Enable 14	
31	Bit 14 Clock Enable 15	
32	Bit 15 Clock Enable 16	

	Clock Enable 2
33	Bit 0 Clock Enable 17
34	Bit 1 Clock Enable 18
35	Bit 2 Clock Enable 19
36	Bit 3 Clock Enable 20
37	Bit 4 Clock Enable 21
38	Bit 5 Clock Enable 22
39	Bit 6 Clock Enable 23
40	Bit 7 Clock Enable 24
41	Bit 8 Clock Enable 25
42	Bit 9 Clock Enable 26
43	Bit 10 Clock Enable 27
44	Bit 11 Clock Enable 28
45	Bit 12 Clock Enable 29
46	Bit 13 Clock Enable 30
47	Bit 14 Clock Enable 31
48	Bit 15 Clock Enable 32
	Clock Enable 3
49	Bit 0 Clock Enable 33
50	Bit 1 Clock Enable 34
51	Bit 2 Clock Enable 35
52	Bit 3 Clock Enable 36
53	Bit 4 Clock Enable 37
54	Bit 5 Clock Enable 38
55	Bit 6 Clock Enable 39
56	Bit 7 Clock Enable 40
57	Bit 8 Clock Enable 41
58	Bit 9 Clock Enable 42
59	Bit 10 Clock Enable 43
60	Bit 11 Clock Enable 44
61	Bit 12 Clock Enable 45
62	Bit 13 Clock Enable 46
63	Bit 14 Clock Enable 47
64	Bit 15 Clock Enable 48
	Clock Enable 4
65	Bit 0 Clock Enable 49
66	Bit 1 Clock Enable 50
67	Bit 2 Clock Enable 51
68	Bit 3 Clock Enable 52
69	Bit 4 Clock Enable 53
70	Bit 5 Clock Enable 54
71	Bit 6 Clock Enable 55
72	Bit 7 Clock Enable 56
73	Bit 8 Clock Enable 57
74	Bit 9 Clock Enable 58
75	Bit 10 Clock Enable 59
76	Bit 11 Clock Enable 60
77	Bit 12 Clock Enable 61
78	Bit 13 Clock Enable 62
79	Bit 14 Clock Enable 63

80	Bit 15 Reserved
81-96	Reserved

Bit Numbering

The following represents the hexadecimal and decimal value for each bit in the 16 bit MODBUS register.

Bit Number	Hex Value	Decimal Value
0	0x0001	1
1	0x0002	2
2	0x0004	4
3	0x0008	8
4	0x0010	16
5	0x0020	32
6	0x0040	64
7	0x0080	128
8	0x0100	256
9	0x0200	512
10	0x0400	1024
11	0x0800	2048
12	0x1000	4096
13	0x2000	8192
14	0x4000	16384
15	0x8000	32768

LSB – Least significant byte – bits 0-7
MSB – Most significant byte – bits 8-15

Sample Project Data Map

This section provides a sample register map for the most commonly required data for a 1-chamber precipitator, 4 fields deep with one T/R controller per field. One rapper control is configured along with one energy management system. The CAN-Transceiver ID is programmed for 1.

Tag Name	Modbus Address	Units	Description
AVCs (TR Controls)	ID=1		
U01_MTC01_SW1	40201		Status word 1
U01_MTC01_SW2	40202		Status word 2
U01_MTC01_AW1	40204		Alarm word
U01_MTC01_PV	40207	Volts	Primary voltage
U01_MTC01_PI	40208	Amps	Primary current
U01_MTC01_PP	40209	kW	Primary power
U01_MTC01_SV1	40210	kV	Secondary voltage
U01_MTC01_SV2	40211	kV	Secondary voltage
U01_MTC01_SI	40212	ma	Secondary current
U01_MTC01_SPM	40213	spm	Sparks per minute
U01_MTC01_APM	40214	apm	Arcs per minute
U01_MTC01_CW1	40301		Control word
U01_MTC01_PVL	40304	Volts	Primary volt limit
U01_MTC01_PIL	40305	Amps	Primary current limit
U01_MTC01_SVL	40306	kV	Secondary volt limit
U01_MTC01_SIL	40307	ma	Secondary current limit
U01_MTC02_SW1	40401		Status word 1
U01_MTC02_SW2	40402		Status word 2
U01_MTC02_AW1	40404		Alarm word
U01_MTC02_PV	40407	Volts	Primary voltage
U01_MTC02_PI	40408	Amps	Primary current
U01_MTC02_PP	40409	kW	Primary power
U01_MTC02_SV1	40410	kV	Secondary voltage
U01_MTC02_SV2	40411	kV	Secondary voltage
U01_MTC02_SI	40412	ma	Secondary current
U01_MTC02_SPM	40413	spm	Sparks per minute
U01_MTC02_APM	40414	apm	Arcs per minute
U01_MTC02_CW1	40501		Control word
U01_MTC02_PVL	40504	Volts	Primary volt limit
U01_MTC02_PIL	40505	Amps	Primary current limit
U01_MTC02_SVL	40506	kV	Secondary volt limit
U01_MTC02_SIL	40507	ma	Secondary current limit
U01_MTC03_SW1	40601		Status word 1
U01_MTC03_SW2	40602		Status word 2
U01_MTC03_AW1	40604		Alarm word
U01_MTC03_PV	40607	Volts	Primary voltage
U01_MTC03_PI	40608	Amps	Primary current
U01_MTC03_PP	40609	kW	Primary power

U01_MTC03_SV1	40610	kV	Secondary voltage
U01_MTC03_SV2	40611	kV	Secondary voltage
U01_MTC03_SI	40612	ma	Secondary current
U01_MTC03_SPM	40613	spm	Sparks per minute
U01_MTC03_APM	40614	apm	Arcs per minute
U01_MTC03_CW1	40701		Control word
U01_MTC03_PVL	40704	Volts	Primary volt limit
U01_MTC03_PIL	40705	Amps	Primary current limit
U01_MTC03_SVL	40706	kV	Secondary volt limit
U01_MTC03_SIL	40707	ma	Secondary current limit
U01_MTC04_SW1	40801		Status word 1
U01_MTC04_SW2	40802		Status word 2
U01_MTC04_AW1	40804		Alarm word
U01_MTC04_PV	40807	Volts	Primary voltage
U01_MTC04_PI	40808	Amps	Primary current
U01_MTC04_PP	40809	kW	Primary power
U01_MTC04_SV1	40810	kV	Secondary voltage
U01_MTC04_SV2	40811	kV	Secondary voltage
U01_MTC04_SI	40812	ma	Secondary current
U01_MTC04_SPM	40813	spm	Sparks per minute
U01_MTC04_APM	40814	apm	Arcs per minute
U01_MTC04_CW1	40901		Control word
U01_MTC04_PVL	40904	Volts	Primary volt limit
U01_MTC04_PIL	40905	Amps	Primary current limit
U01_MTC04_SVL	40906	kV	Secondary volt limit
U01_MTC04_SIL	40907	ma	Secondary current limit

Energy Management System (EMS)	ID=2		
Opacity	40101	%	Stack Opacity
Opacity_StatusWord	40104		Opacity Status
EMS_ControlWord	40105		EMS control word
EMS_LowerLimit	40107	%	Lower opacity limit
EMS_UpperLimit	40108	%	Upper opacity limit
EMS_Value_Field1	40118		Power value for field 1
EMS_Value_Field2	40124		Power value for field 2
EMS_Value_Field3	40130		Power value for field 3
EMS_Value_Field4	40136		Power value for field 4

Rapper Control (MRC)	ID=3		
U01_MRC_SW1	40001		Status word 1
U01_MRC_SW2	40002		Status word 2
U01_FIRE_1	40003		Rapper firing indication
U01_Program_Num_Status	40006		Program number (read only)
U01_MRC_CW	40201		MRC control word
U01_Program_Num_Set	40207		Program number (read/write)
U01_CYC_HR_A_1	40209	hour	Cycle clock hours
U01_CYC_SEC_A_1	40210	seconds	Cycle clock seconds
U01_CYC_HR_A_2	40213	hour	Cycle clock hours
U01_CYC_SEC_A_2	40214	seconds	Cycle clock seconds

U01_CYC_HR_A_3	40217	hour	Cycle clock hours
U01_CYC_SEC_A_3	40218	seconds	Cycle clock seconds
U01_CYC_HR_A_4	40221	hour	Cycle clock hours
U01_CYC_SEC_A_4	40222	seconds	Cycle clock seconds
U01_CYC_HR_A_5	40225	hour	Cycle clock hours
U01_CYC_SEC_A_5	40226	seconds	Cycle clock seconds
U01_CYC_HR_A_6	40229	hour	Cycle clock hours
U01_CYC_SEC_A_6	40230	seconds	Cycle clock seconds
U01_CYC_HR_A_7	40233	hour	Cycle clock hours
U01_CYC_SEC_A_7	40234	seconds	Cycle clock seconds
U01_CYC_HR_A_8	40237	hour	Cycle clock hours
U01_CYC_SEC_A_8	40238	seconds	Cycle clock seconds

MODBUS Register Sample Data

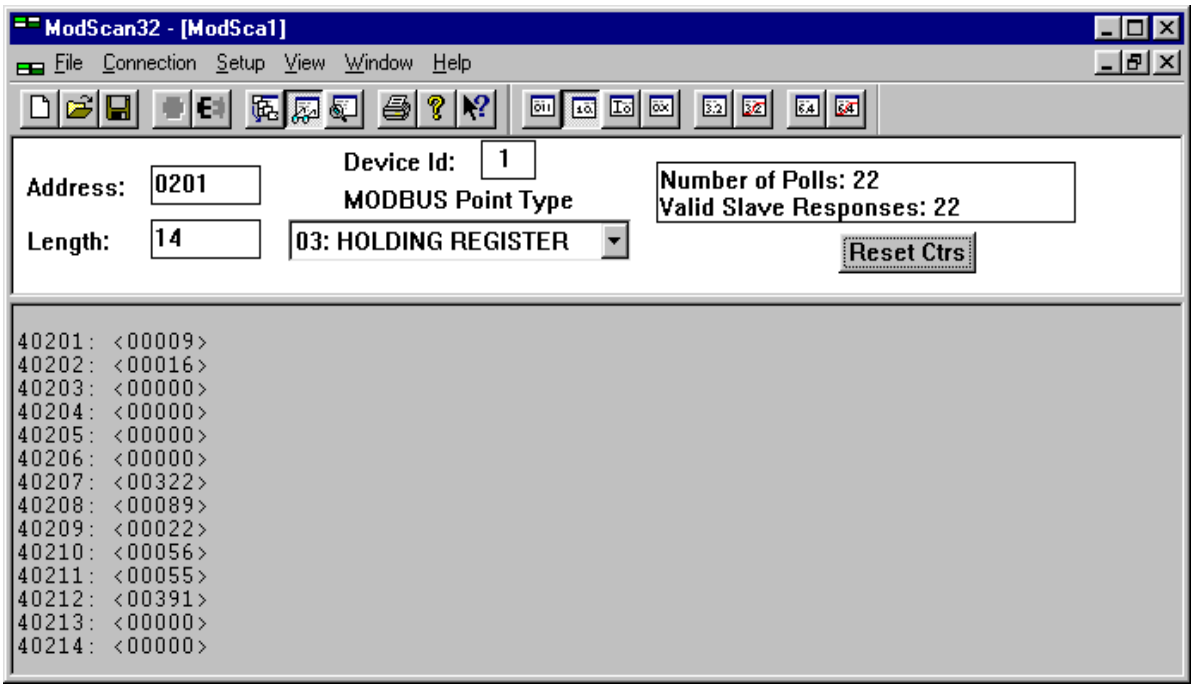
This section shows a sample printout of MODBUS registers as they were read from a CAN-Transceiver.

Below is a screen capture of a program that functions as a MODBUS master on a PC communicating with the CAN-Transceiver.

The program has been setup as follows:

Device Id	1	CAN-Transceiver ID selected in the ID Setup prompt
Address	201	Starting MODBUS register to scan. Starts with AVC status register
Length	14	Number of registers to scan

Register/Command type: 03: Read Holding registers

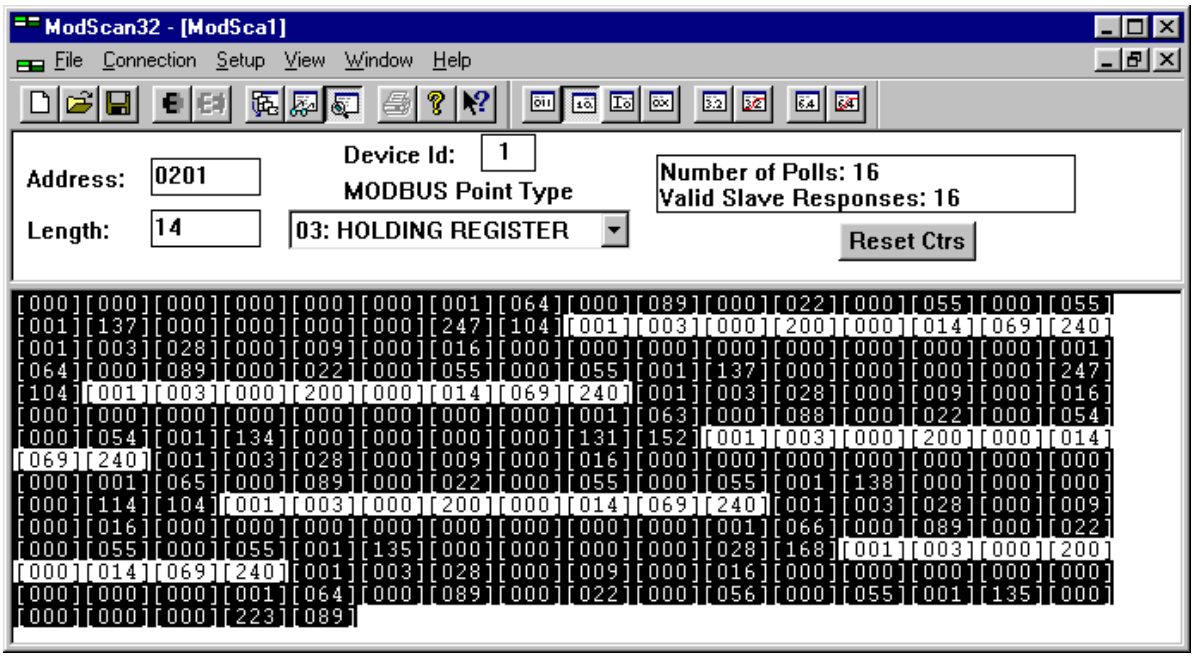


The interpretation of the data display is as follows:

Address	Register Value	Definition	
40201	<0009>	AVC Status Word 1	Device is running in continuous mode
40202	<0016>	AVC Status Word 2	Is limit operational (0010 hex)
40203	<0000>	Reserved	
40204	<0000>	Alarm word	No alarms
40205	<0000>	Reserved	
40206	<0000>	Reserved	
40207	<0322>	Primary voltage	322 Volts
40208	<0089>	Primary current	89 Amps
40209	<0022>	Primary power	22 kW
40210	<0056>	Secondary voltage 1	56 kV

40211	<0055>	Secondary voltage 2	55 kV
40212	<0391>	Secondary current	391 ma
40213	<0000>	Sparks per minute	0
40214	<0000>	Arcs per minute	0

The program is also capable of showing the serial traffic to and from a MODBUS device.



MODSCAN32 is an application developed by Win-Tech Software Design. A free trial demo is available for download from www.win-tech.com.